AMENDMENTS TO THE DRAWINGS:

In the Office Action, the Examiner objected to the drawings and in particular to the orientation of the primary crystal grain boundaries illustrated in FIG. 6. In order to overcome these objections, a replacement figure is submitted herewith. In FIG. 6, the primary crystal grain boundaries appear within the range noted by the Examiner. Approval of these changes to the Drawings is respectfully requested.

REMARKS

Claims 1, 5-7, 11 and 12 have been amended. Claims 1-14 are pending and under consideration. Claims 1, 7, 13 and 14 are the independent claims. No new matter is presented in this Amendment. Proper support for the amendment to claims 5, 6, 11 and 12 can be found in the specification at least at paragraph [0032].

INFORMATION DISCLOSURE STATEMENT

In the Office Action, it is noted that the IDS filed May 25, 2006 fails to comply with 37 C.F.R. § 1.98(a)(2) by indicating that a legible copy is required. Although Applicants believe that a legible copy of the document was submitted on May 25, 2006, enclosed herewith is another legible copy of the document cited in the IDS filed May 25, 2006.

Accordingly, Applicants respectfully request that the Examiner considered these documents.

DRAWINGS

The drawings are objected to under 37 CFR 1.83(a).

Applicants submit herewith a replacement sheet of FIG. 6 correcting the minor objections noted in the Office Action.

Approval of these changes to the Drawings is respectfully requested.

REJECTIONS UNDER 35 U.S.C. §112:

Claims 5, 6, 11 and 12 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants have amended claims 5, 6, 11 and 12 in accordance with the Examiner's comments and assert that claims 5, 6, 11 and 12, as amended, fully comply with the requirements of 35 U.S.C. §112, second paragraph.

Accordingly, Applicants respectfully request that the rejection of claims 5, 6, 11 and 12 under 35 U.S.C. §112, second paragraph, be withdrawn.

REJECTIONS UNDER 35 U.S.C. §102:

Claims 1, 2, 4, 7, 8, and 10 are rejected under 35 U.S.C. §102(e) as being anticipated by Isobe et al. (U.S. Patent 6,890,840).

Applicants respectfully traverse this rejection for at least the following reasons.

Regarding the rejection of independent claim 1, it is noted that claim 1 recites a thin film transistor (TFT) **comprising** a lightly doped drain (LDD) region or offset region and **a plurality of primary crystal grain boundaries**, wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are **not positioned in the LDD or offset region**.

The Office Action states that Isobe discloses a TFT comprising an LDD region wherein the TFT is formed so that primary crystal grain boundaries of a polysilicon substrate are not positioned in the LDD region. Isobe in particular discloses that the crystal aggregate boundaries are located outside of the TFT formation region (column 6, lines 29-34). The Office Action further states that it is considered that the aggregate boundaries are the primary grain boundaries, and therefore, since there are no primary grain boundaries in the TFT region, there cannot be any primary grain boundaries in the LDD region.

However, a review of Isobe shows the formation of a channel formation region, or a TFT formation region, using one crystal aggregate (domain) by controlling crystal location and size, thus suppressing TFT variations. Each TFT formation region is isolated, a metallic element for promoting crystallization (typically Ni) is added, and heat treatment is performed, thus making it possible to arbitrarily determine the locations of crystal aggregates (domains) (abstract). In other words, Isobe discloses a method for forming a channel formation region using a metal induced lateral crystallization (MILC) method. It is noted that in the MILC method, a solid-state crystallization technique, amorphous silicon does not solidify but rather crystallization results from realignment of molecules in the solid state, and thus primary grain boundaries are not formed. Accordingly, in Isobe crystal aggregate boundaries are eliminated not only from the TFT formation regions but from the TFT itself.

Furthermore, contrary to Isobe, an aspect of the present invention teaches that the polysilicon substrate is formed by a sequential lateral solidification (SLS) method. In the SLS method, amorphous silicon crystallizes while it solidifies, crystal grains collide with each other while forming due to different densities between the liquid and solid states, and the colliding crystal grains push each other upward due to expansion in volume to form a primary crystal grain boundary. Accordingly, the crystal grains formed by the MILC crystallization method taught by Isobe are different from the crystal grains formed by the SLS crystallization method taught by an aspect of the present invention.

Therefore, since Isobe discloses an MILC method and as noted above in the MILC method no primary crystal grain boundaries are formed, Isobe does not teach or suggest a TFT comprising a plurality of primary crystal grain boundaries, as recited in independent claim 1.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. § 102(e) should be withdrawn because Isobe fails to teach or suggest each feature of independent claim 1.

Furthermore, Applicants respectfully assert that dependent claims 2 and 4 are allowable at least because of their dependence from claim 1, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 2 and 4 also distinguish over the prior art.

Regarding the rejection of claim 7, it is noted that claim 7 recites a flat panel display device comprising: **a thin film transistor comprising**: an LDD region or offset region, and **a plurality of primary crystal grain boundaries**, wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are not positioned in the LDD or offset region.

As noted above, Isobe shows the formation of a channel formation region, or a TFT formation region, using one crystal aggregate (domain) by controlling crystal location and size, thus suppressing TFT variations (abstract). In other words, Isobe discloses a method for forming a channel formation region using a metal induced lateral crystallization (MILC) method in which crystal aggregate boundaries are eliminated not only from the TFT formation regions but from the TFT itself. As also noted above, in the MILC method, a solid-state crystallization technique, amorphous silicon does not solidify but rather crystallization results from realignment

of molecules in the solid state, and thus primary grain boundaries are not formed. Therefore, Isobe does not teach or suggest a TFT comprising a plurality of primary crystal grain boundaries, as recited in independent claim 7, since Isobe eliminates the boundaries altogether which is the purpose of the MILC method.

Accordingly, Applicants respectfully assert that the rejection of claim 7 under 35 U.S.C. § 102(e) should be withdrawn because Isobe fails to teach or suggest each feature of independent claim 7.

Furthermore, Applicants respectfully assert that dependent claims 8 and 10 are allowable at least because of their dependence from claim 7, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 8 and 10 also distinguish over the prior art.

Claims 1, 4-6 and 10-14 are rejected under 35 U.S.C. §102(e) as being anticipated by Lee (U.S. Patent 6,720,587).

Applicants respectfully traverse this rejection for at least the following reasons.

Regarding the rejection of independent claim 1, it is noted that claim 1 recites a thin film transistor (**TFT**) **comprising** a lightly doped drain (LDD) region or offset region and **a plurality of primary crystal grain boundaries**, wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are **not positioned in the LDD or offset region**.

The Office Action relies on FIG. 8 of Lee for a teaching of an LCD comprising a TFT comprising an offset region (gate insulator), wherein the primary grain boundaries are positioned in various regions but not in the offset region. The Office Action further states that the gate insulator **can be considered** the offset region since it "offsets" the gate from the channel.

Applicants respectfully traverse such characterization for the following reasons. Lee discloses a TFT comprising drain, source and gate regions wherein a distance between channels of each TFT comprising dual or multiple channels has a particular relation according to a disclosed equation (column 3, lines 38-57). Lee does not teach or suggest the location or the existence of a gate insulator, or an offset region, as alleged in the Office Action.

Without any support or evidence of why or how the gate insulator can be considered the offset region, it appears the Examiner is relying on his personal knowledge for such assertion or is taking Office Notice. However, by taking Official Notice, the rejection is being based, in part, on the personal knowledge of the Examiner. The personal knowledge of the Examiner, when used as a basis for a rejection, must be supported by an affidavit as to the specifics of the facts of that knowledge when called for by the applicant. See, MPEP 2144.03, 37 C.F.R. § 1.104(d)(2). In short, the rules of the U.S. Patent and Trademark Office require that the Examiner must either support this assertion with an Affidavit, or withdraw the rejection. Therefore, it is further respectfully requested that the Examiner support the rejection with either an affidavit or a reference, or withdraw the rejection.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. § 102(e) should be withdrawn because Lee fails to teach or suggest each feature of independent claim 1.

Furthermore, Applicants respectfully assert that dependent claims 4-6 are allowable at least because of their dependence from claim 1, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 4-6 also distinguish over the prior art.

Regarding the rejection of independent claim 13, it is noted that claim 13 recites a thin film transistor (TFT) comprising a lightly doped drain (LDD) region or offset region, wherein the thin film transistor is formed so that primary crystal grain boundaries of a polysilicon substrate are positioned in channel, source and drain regions but not positioned in the LDD or offset region.

As noted above, the Office Action relies on FIG. 8 of Lee for a teaching of an LCD comprising a TFT comprising an offset region (gate insulator), wherein the primary grain boundaries are positioned in various regions but not in the offset region. The Office Action further states that the gate insulator can be considered the offset region since it "offsets" the gate from the channel. As also noted above, Applicants respectfully traverse such characterization since Lee does not teach or suggest the location or the existence of a gate insulator or an offset region, as alleged in the Office Action.

Accordingly, Applicants respectfully assert that the rejection of claim 13 under 35 U.S.C.

§ 102(e) should be withdrawn because Lee fails to teach or suggest each feature of independent claim 13.

Regarding the rejection of independent claim 14, it is noted that claim 14 recites a flat panel display device comprising: a thin film transistor including an LDD region or offset region, wherein the thin film transistor is formed so that primary crystal grain boundaries of a polysilicon substrate are positioned in channel, source and drain regions but not positioned in the LDD or offset region.

As noted above, Lee does not teach or suggest the location or the existence of a gate insulator or an offset region, as alleged in the Office Action.

Accordingly, Applicants respectfully assert that the rejection of claim 14 under 35 U.S.C. § 102(e) should be withdrawn because Lee fails to teach or suggest each feature of independent claim 14.

Regarding the rejection of claims 10-12 it is noted that these claims depend from independent claim 7. However, it is noted that claim 7 does not stand rejected by Lee. Accordingly, since Lee does not anticipate claim 7 upon which claims 10-12 depend, Applicants respectfully request that the rejection of claims 10-12 under 35 U.S.C. § 102(e) be withdrawn because Lee fails to teach or suggest each feature of independent claim 7, upon which claims 10-12 depend from and because they include additional features which are not taught or suggested by the prior art.

REJECTIONS UNDER 35 U.S.C. §103:

Claims 1-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Zhang et al. (U.S. Patent 5,563,426 in view of Suzuki et al. (U.S. Patent 6,274,888).

Regarding the rejection of independent claim 1, it is noted that claim 1 recites a thin film transistor (**TFT**) **comprising** a lightly doped drain (LDD) region or offset region and **a plurality of primary crystal grain boundaries**, wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are **not positioned in the LDD or**

offset region.

The Office Action states that Zhang discloses a TFT formed so that primary crystal grain boundaries 4 of a polysilicon substrate are formed outside the TFT formation regions (FIGS. 1B, 1C and 4C). The Office Action recognizes that Zhang fails to teach an LDD region and relies on Suzuki for such teaching. Applicants respectfully assert that the combination of Zhang and Suzuki fails to disclose each of these features and furthermore there is no teaching or suggestion to combine these references to teach the feature of independent claim 1.

Zhang discloses a method of manufacturing a TFT using a crystal silicon film obtained by crystallizing an amorphous silicon film using a plurality of island nickel films (column 11, lines 21-22). The TFT includes island nickel regions 2, portions 3, inter-crystalline boundaries 4, an intermediate region 5, a semiconductor region 6 and a gate wire 7 (column 12, lines 25-55; FIGS. 1A-1C). In other words, Zhang discloses a method of manufacturing a TFT using metal induce lateral crystallization (MILC), that is, Zhang teaches a method in which primary grain boundaries are eliminated altogether from the device, since the method taught by Zhang produces a structure similar to a monocrystal (column 5, lines 66-67). Therefore, the alleged inter-crystalline boundaries 4, as suggest in the Office Action, are not primary boundaries but rather grooves (column 12, lines 41-43). Accordingly, Zhang fails to teach or suggest the features recited in independent claim 1.

Suzuki discloses a TFT also manufactured by the MILC method, in which large grains are formed thus avoiding the formation of primary crystal grain boundaries (column 9, lines 5-17). Therefore, Suzuki also fails to teach or suggest a thin film transistor formed so that **primary crystal grain boundaries** of a polysilicon substrate are not positioned in the LDD or offset region, as recited in independent claim 1.

Accordingly, Applicants respectfully assert that the rejection of claim 1 under 35 U.S.C. § 103(a) should be withdrawn because neither Zhang nor Suzuki, whether taken singly or combined, teach or suggest each feature of independent claim 1.

Furthermore, Applicants respectfully assert that dependent claims 2-6 are allowable at least because of their dependence from claim 1, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 2-6 also distinguish over the prior art.

Regarding the rejection of claim 7, it is noted that claim 7 recites a flat panel display device comprising: **a thin film transistor comprising**: an LDD region or offset region, and **a plurality of primary crystal grain boundaries**, wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are not positioned in the LDD or offset region.

As noted above, neither Zhang nor Suzuki, whether taken singly or combined teach or suggest **a plurality of primary crystal grain boundaries**, wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are not positioned in the LDD or offset region.

Accordingly, Applicants respectfully assert that the rejection of claim 7 under 35 U.S.C. § 102(e) should be withdrawn because neither Zhang nor Suzuki, whether taken singly or combined teach or suggest each feature of independent claim 7.

Furthermore, Applicants respectfully assert that dependent claims 9-12 are allowable at least because of their dependence from claim 7, and because they include additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that claims 9-12 also distinguish over the prior art.

CONCLUSION:

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

STEIN, MCEWEN & BUI, LLP

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